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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Before the Board of Patent Appeals and Interferences

In re the Application		
Inventor	:	SETHURAMAN
Application No.	:	10/530,495
Filed	:	04/06/2005
For	:	DATA PROCESSING APPARATUS ADDRESS RANGE DEPENDENT PARALLELIZATION OF INSTRUCTIONS

APPEAL BRIEF

On Appeal from Group Art Unit 2183

Date: 08/04/2007

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Michael Ure
(Name)

8/7/07
(Signature and Date)

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I. REAL PARTY IN INTEREST

The real party in interest is NXP B.V., the successor in interest to the present assignee of record of the present application, Koninklijke Philips Electronics N.V., and not the party named in the above caption.

II. RELATED APPEALS AND INTERFERENCES

With regard to identifying by number and filing date all other appeals or interferences known to Appellant which will directly effect or be directly affected by or have a bearing on the Board's decision in this appeal, Appellant is not aware of any such appeals or interferences.

III. STATUS OF CLAIMS

Claims 1-17 are pending, of which claims 1-12 and 14-17 stand finally rejected and form the subject matter of the present appeal. Claim 13 has been canceled.

IV. STATUS OF AMENDMENTS

All amendments have been entered. No amendment after final rejection has been submitted.

V. SUMMARY of the CLAIMED SUBJECT MATTER

The present invention relates to a data processing apparatus in which the way the instruction execution unit parallelizes processing of instructions depends on a detected address range in which the instruction address lies. As described more particularly at

page 2, lines 18-26 of the specification, the instruction execution unit may treat information from the instruction memory as relatively longer instruction words, containing relatively more instructions, when these words come from a range of addresses that refer to instructions from the inner loop of a program; and the instruction execution may treat the information as relatively shorter instruction words, containing relatively fewer instructions, when these words come from another range of addresses. Thus, high parallelism can be realized in the inner loop and high storage efficiency can be realized outside the inner loop, without need for explicit instructions to change the instruction word length when passing into or out of the inner loop. The greater the number of instructions in an instruction word, the greater the likelihood of having to include "no-operation" instructions, reducing storage efficiency.

The following analysis of independent claim 1 is presented for convenience:

Element	Figure(s)	Paragraph(s) and/or page(s)
1. A data processing apparatus, the apparatus comprising:		
an instruction address generation circuit for outputting an instruction address;	Fig. 1, 10	Page 3, line 31 to page 4, line 11
an instruction memory system arranged to output an instruction word addressed by the instruction address;	Fig. 1, 12; Fig. 2, 12; Fig. 2A, 204; Fig. 2B, 204; Fig. 6, 60; Fig. 7, 60.	Page 3, line 31 to page 4, line 11; page 6, line 27 to page 9, line 2; page 11, line 20 to page 12, line 6; page 12, lines 7-23.
an instruction execution unit, arranged to process a plurality of instructions from the instruction word in parallel;	Fig. 1, 14; Fig. 2A, 200; Fig. 2B, 200; Fig. 7, 70.	Page 3, line 31 to page 4, line 11; page 6, line 27 to page 9, line 2; page 12, lines 7-23.

a detection unit, arranged to detect in which of a plurality of ranges the instruction address lies,	Fig. 1, 16; Fig. 3; Fig. 6, 66.	Page 3, line 31 to page 4, line 11; page 9, line 3 to page 10, line 8; page 11, line 20 to page 12, line 6.
the detection unit being coupled to the instruction execution unit and/or the memory system, to control a way in which the instruction execution unit parallelizes processing of the instructions from the instruction word, dependent on a detected range..	Fig. 1, Fig. 2, Fig. 2A, Fig. 2B, Fig. 6	Page 4, line 28 to page 5, line 5; page 6, line 27 to page 9, line 2; page 11, line 20 to page 12, line 6.

The following analysis of independent claim 15 is presented for convenience:

Element	Figure(s)	Paragraph(s) and/or page(s)
15. A method of executing a program with data processing apparatus, the method comprising:		
using an instruction address to fetch an instruction word;	Fig. 1, 10	Page 3, line 31 to page 4, line 11
executing instructions from the fetched instruction word;	Fig. 1, 14; Fig. 2A, 200; Fig. 2B, 200; Fig. 7, 70.	Page 3, line 31 to page 4, line 11; page 6, line 27 to page 9, line 2; page 12, lines 7-23.
detecting in which of a plurality of ranges the instruction address lies,	Fig. 1, 16; Fig. 3; Fig. 6, 66.	Page 3, line 31 to page 4, line 11; page 9, line 3 to page 10, line 8; page 11, line 20 to page 12, line 6.
controlling a way in which the instruction execution is parallelized dependent on a detected range.	Fig. 1, Fig. 2, Fig. 2A, Fig. 2B, Fig. 6	Page 4, line 28 to page 5, line 5; page 6, line 27 to page 9, line 2; page 11, line 20 to page 12, line 6.

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VI. GROUNDS of REJECTION to be REVIEWED ON APPEAL

The issues in the present matter are whether:

1. under 35 USC 103(a), claims 1-5, 7 and 15-17 are unpatentable over Fisher in view of Barry.
2. under 35 USC 103(a), claims 8 and 9 are unpatentable over Fisher in view of Barry and further in view of Maiyuran.
3. under 35 USC 103(a), claims 10 and 12 are unpatentable over Fisher in view of Barry and further in view of Sanches.
4. under 35 USC 103(a), claim 11 is unpatentable over Fisher in view of Barry and further in view of Sanches and further still in view of Maiyuran.

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VII. ARGUMENT

I. Rejection of Claims 1-5, 7 and 15-17 as Being Unpatentable Over Fisher in View of Barry

Applicant refers in particular to pages 16 and 17 of the final rejection. Here, the rejection argues as follows:

1. Fisher teaches controlling a way in which instruction execution is parallelized in response to interrupts.
2. Barry teaches detecting an instruction address range and generating an interrupt.
3. *Therefore*, it would have been obvious to detect an instruction address range and control a way in which instruction execution is parallelized dependent on a detected range.

Even assuming points 1 and 2 to be true, point 3 simply does not follow.

Clearly, interrupts can be generated for many different purposes. Fisher and Barry share no common purpose. Their "linking" teaching is the use of interrupts (for different purposes). Such a weak link is insufficient to support a case of obviousness.

Fisher clearly teaches identifying a process as a low ILP (Instruction Level Parallelism) or high ILP process in *process tables* of the operating system of the CPU. In response to an interrupt, the process tables are consulted and the ILP mode is set accordingly. (Fisher, col. 6, lines 37-47.)

Setting speculation aside, Barry does not contain any clear teaching that would alter that arrangement. As described in Barry, address range detection is used principally for purposes of debugging.

Accordingly, claims 1-5, 7 and 15-17 would not have been obvious given Fisher and Barry.

II. Rejection of Claims 8 and 9 as Being Unpatentable Over Fisher in View of Barry and Further in View of Maiyuran

Maiyuran was cited in relation to disabling the supply of clock signals to a memory unit when an address in the range of a different memory unit is detected.

Maiyuran actually teaches something quite different. That is, Maiyuran teaches power management of a cache memory on a *microinstruction-by-microinstruction* basis. The scheme of Maiyuran may be seen in Table 1 of col. 2 of Maiyuran. As summarized in paragraph [0030], "By disabling cache components such as ways, tag fields 120, data fields 130, state fields S and LRUs 170 on a UOP-by-UOP basis, the cache architecture 100 achieves considerable power conservation over known alternatives."

Extrapolation of the teachings of Maiyuran to teach "disabling the supply of clock signals to selected memory modules as appropriate" (or as the Examiner may choose) is unwarranted.

III. Rejection of Claims 10 and 12 as Being Unpatentable Over Fisher in View of Barry and Further in View of Sanches

Sanches was cited in relation to the feature of the instruction memory supplying the instruction word as a combination of instructions from memory units in whose respective range the instruction address lies. This feature is illustrated in Figures 6 and 7 and described on pages 11 and 12 of the present specification.

Sanches is not believed to teach or suggest any such feature.

In Sanches, Figure 2 thereof, an address management circuit IAC computes respective addresses a0-a3 for *each* of the respective memory banks M0-M3 in response to *each* program counter (PC) value according to an algorithm A1 (paragraphs [0055] to [0061]). There is no question of address ranges of the memory banks, nor is there any possibility of those (non-existent) ranges overlapping, except to consider that all of the memory banks have the identical range and overlap completely. The latter interpretation is not a reasonable one.

IV. Rejection of Claim 11 as Being Unpatentable Over Fisher in View of Barry Further in View of Sanches and Further Still in View of Maiyuran

The rejection of claim 11 is believed to be flawed for similar reasons as the rejections addressed in preceding Sections III. and IV.

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VIII. CONCLUSION

In view of the above analysis, it is respectfully submitted that the referenced teachings, whether taken individually or in combination, fail to anticipate or render obvious the subject matter of any of the present claims. Therefore, reversal of all outstanding grounds of rejection is respectfully solicited.

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IX. APPENDIX: THE CLAIMS ON APPEAL

1. A data processing apparatus, the apparatus comprising an instruction address generation circuit for outputting an instruction address; an instruction memory system arranged to output an instruction word addressed by the instruction address; an instruction execution unit, arranged to process a plurality of instructions from the instruction word in parallel; a detection unit, arranged to detect in which of a plurality of ranges the instruction address lies, the detection unit being coupled to the instruction execution unit and/or the instruction memory system, to control a way in which the instruction execution unit parallelizes processing of the instructions from the instruction word, dependent on a detected range.

2. A data processing apparatus according to claim 1, wherein the instruction execution unit and/or the instruction memory system is arranged to adjust a width of the instruction word that determines a number of instructions from the instruction word that is processed in parallel, dependent on the detected range.

3. A data processing apparatus according to claim 1, wherein the instruction execution unit comprises a plurality of functional units, the instruction execution unit being arranged to select a subset of the functional units that is available for processing the instructions, dependent on the detected range.

4. A data processing apparatus according to claim 1, wherein the instruction execution

unit comprises a plurality of functional units, the instruction execution unit being arranged to select whether functional units or groups of functional units from a set of functional units each receive respective instructions from the instruction word, or receive a shared instruction from the instruction word, dependent on the detected range.

5. A data processing apparatus according to claim 2, wherein the instruction memory comprises a first memory unit and a second memory unit, providing storage with a first and second unit of width of addressable memory locations for instruction words of different lengths with addresses in a first and second range respectively, the first and second unit of width being mutually different.

6. A data processing apparatus according to claim 5, programmed to execute a program, relatively longer instruction words from an inner loop of the program being stored in the first memory unit, relatively shorter instruction words from a majority of the program outside the inner loop being stored in the second memory unit, the first unit of width being larger than the second unit of width.

7. A data processing apparatus according to claim 5, comprising a memory mapping unit arranged to map the instruction address onto the first memory unit or the second memory unit, dependent on the detected range.

8. A data processing apparatus according to claim 5, wherein the instruction memory system is arranged to disable supply of clock signals to the first memory unit when

addresses in the second range are detected.

9. A data processing apparatus according to claim 5, wherein the instruction memory system is arranged to disable supply of clock signals to all but the memory unit from whose address range addresses are detected.

10. A data processing apparatus according to claim 2, wherein the instruction memory system comprises a plurality of memory units, each arranged to be responsive to instruction addresses in a respective range, the instruction memory allowing partial overlap of the respective ranges, the instruction memory system being arranged to supply the instruction word as a combination of instructions from those of the memory units in whose respective range the instruction address lies.

11. A data processing apparatus according to claim 10, wherein the instruction memory system is arranged to disable supply of clock signals to at least one of the memory units when the instruction address is not in the respective range of said at least one of the memory units.

12. A data processing apparatus according to claim 10, wherein the execution unit comprises groups of one or more functional units, each group being coupled to a respective predetermined one of the memory units, for receiving instructions from the instruction words, when the instruction address is in the respective range of the respective predetermined one of the memory unit to which the group is coupled.

14. A method of programming a data processing apparatus according to claim 1, the method comprising generating a program of machine instructions for the apparatus; identifying an inner loop of the program; loading the program into the instruction memory system, so that instructions from the inner loop are loaded at memory locations with instruction addresses in a range of addresses for which the apparatus provides a higher degree of parallelism than another range of addresses.

15. A method of executing a program with a data processing apparatus, the method comprising using an instruction address to fetch an instruction word; executing instructions from the fetched instruction word; detecting in which of a plurality of ranges the instruction address lies, controlling a way in which instruction execution is parallelized dependent on a detected range.

16. A method according to claim 15, the method comprising adapting a width of the fetched instruction word dependent on the detected range.

17. A method according to claim 15, the method comprising changing a selection of functional units of the apparatus that is used to execute the instructions dependent on the detected range.

X. APPENDIX: RELATED PROCEEDINGS

NONE

XI. APPENDIX: EVIDENCE

NONE